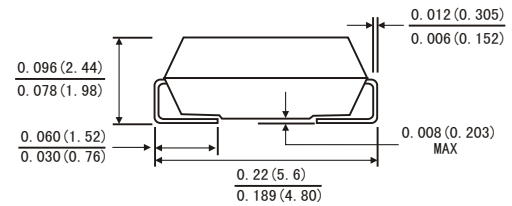
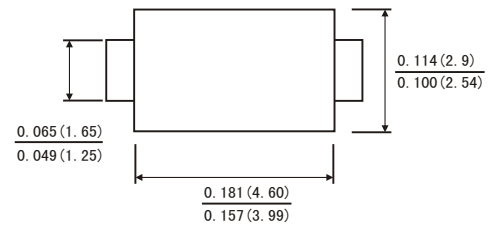


## FEATURES

- For surface mounted applications
- Low profile package
- Glass Passivated Chip Junction
- Superfast reverse recovery time
- Lead free in comply with EU RoHS 2011/65/EU directives



## SMA(DO-214AC)



Dimensions in inches and (millimeters)

## MECHANICAL DATA

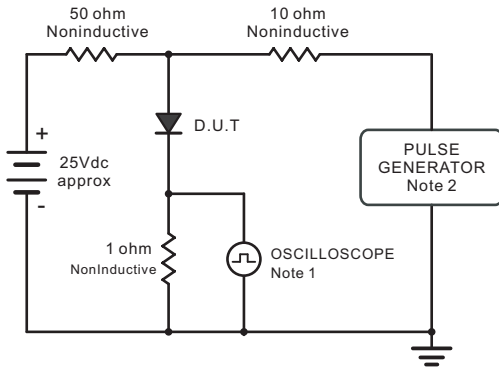
- Case Molded Plastic
- Polarity: Indicated by cathode band
- Weight: 0.002 ounces, 0.064 grams
- Mounting position: Any

## Absolute Maximum Ratings and Characteristics

Ratings at 25 °C ambient temperature unless otherwise specified. Single phase, half wave, 60 Hz, resistive or inductive load. For capacitive load, derate current by 20%.

Parameter	Symbols	ES1A	ES1B	ES1C	ES1D	ES1E	ES1G	ES1J	Units		
Maximum Repetitive Peak Reverse Voltage	$V_{RRM}$	50	100	150	200	300	400	600	V		
Maximum RMS voltage	$V_{RMS}$	35	70	105	140	210	280	420	V		
Maximum DC Blocking Voltage	$V_{DC}$	50	100	150	200	300	400	600	V		
Maximum Average Forward Rectified Current at $T_L = 100\text{ }^\circ\text{C}$	$I_{F(AV)}$	1							A		
Peak Forward Surge Current 8.3 ms Single Half Sine Wave Superimposed on Rated Load (JEDEC Method)	$I_{FSM}$	30							A		
Maximum Forward Voltage at 1 A	$V_F$	1			1.25		1.7		V		
Maximum DC Reverse Current at Rated DC Blocking Voltage $T_a = 25\text{ }^\circ\text{C}$ $T_a = 125\text{ }^\circ\text{C}$	$I_R$	5					100			$\mu\text{A}$	
Typical Junction Capacitance at $V_R = 4\text{V}$ , $f = 1\text{MHz}$	$C_j$	10									pF
Maximum Reverse Recovery Time at $I_F = 0.5\text{A}$ , $I_R = 1\text{A}$ , $I_{rr} = 0.25\text{A}$	$t_{rr}$	35									ns
Operating and Storage Temperature Range	$T_j, T_{stg}$	-55 ~ +150							$^\circ\text{C}$		

Fig.1 Reverse Recovery Time Characteristic And Test Circuit Diagram



Note: 1. Rise Time = 7ns, max.  
Input Impedance = 1megohm, 22pF.  
2. Rise Time = 10ns, max.  
Source Impedance = 50 ohms.

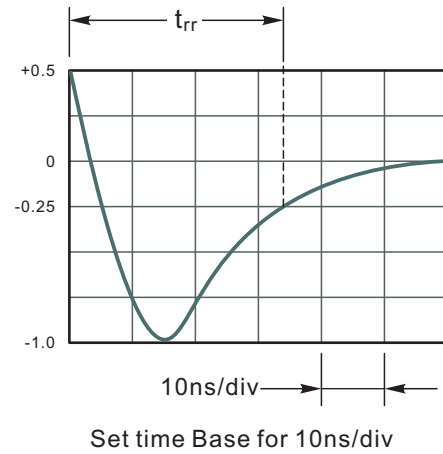


Fig.2 Maximum Average Forward Current Rating

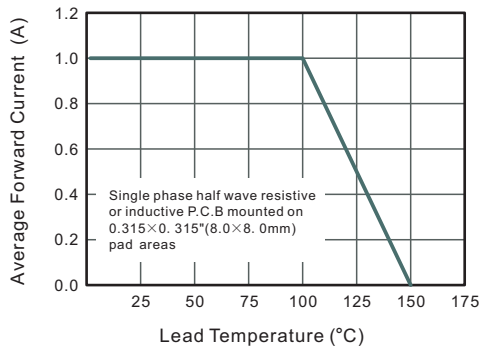


Fig.3 Typical Reverse Characteristics

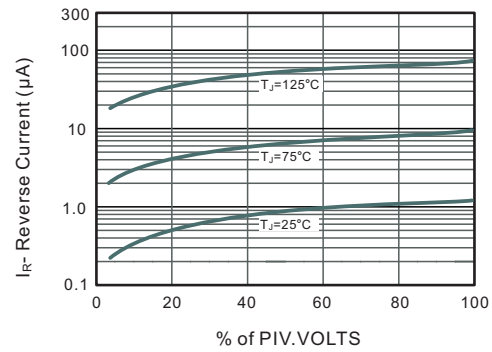


Fig.4 Typical Forward Characteristics

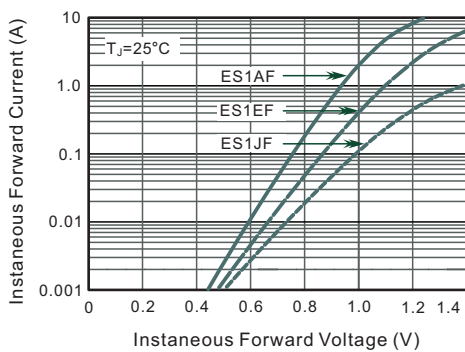


Fig.5 Typical Junction Capacitance

