

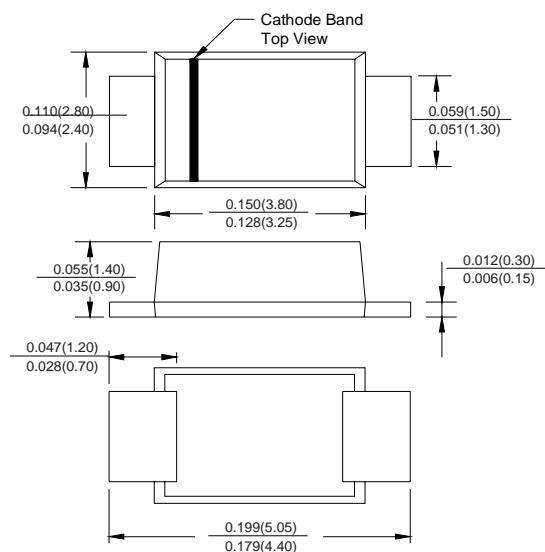


Features

- Glass Passivated Die Construction
- Diffused Junction
- Ultra-Fast Recovery Time for High Efficiency
- Low Forward Voltage Drop, High Current Capability, and Low Power Loss
- Surge Overload Rating to 30A Peak
- Ideally Suited for Automated Assembly
- Plastic Material: UL Flammability Classification Rating 94V-0



SMAF



MECHANICAL DATA

- Case: SMAF
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 27mg 0.00086oz

Dimensions in inches and (millimeters)

Maximum Ratings and Electrical Characteristics

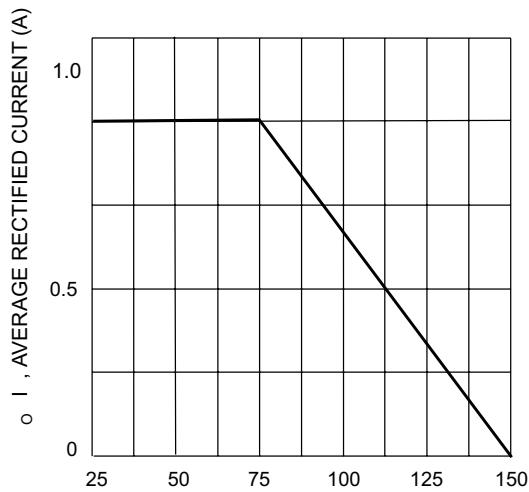
Single phase, half wave, 60Hz, resistive or inductive load.

For capacitive load, derate current by 20%.

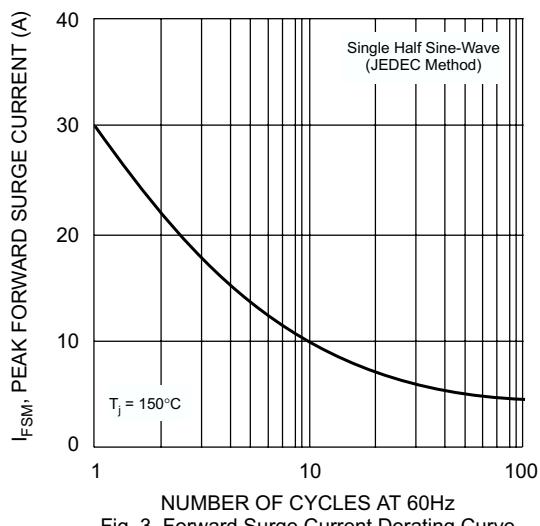
Characteristic	Symbol	US1AF	US1BF	US1DF	US1GF	US1JF	US1KF	US1MF	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V _{RRM} V _{RWM} V _R	50	100	200	400	600	800	1000	V
RMS Reverse Voltage	V _{R(RMS)}	35	70	140	280	420	560	700	V
Average Rectified Output Current @ T _T = 75°C	I _O				1.0				A
Non-Repetitive Peak Forward Surge Current 8.3ms Single half sine-wave Superimposed on Rated Load (JEDEC Method)	I _{FSM}				30				A
Forward Voltage Drop @ I _F = 1.0A	V _{FM}		1.0		1.3		1.7		V
Peak Reverse Current @ T _A = 25°C at Rated DC Blocking Voltage @ T _A = 100°C	I _{RM}				5.0	100			µA
Reverse Recovery Time (Note 2)	t _{rr}		50		75				ns
Typical Junction Capacitance (Note 1)	C _j		20		10				pF
Typical Thermal Resistance, Junction to Terminal	R _{θJT}		30						°C/W
Operating and Storage Temperature Range	T _j , T _{STG}		-65 to +150						°C

Notes:

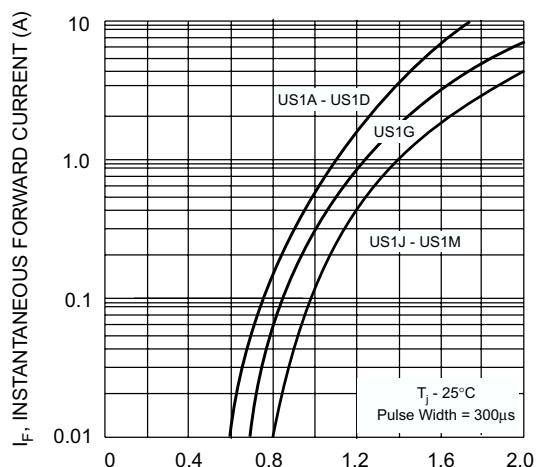
1. Measured at 1.0MHz and applied reverse voltage of 4.0V DC.
2. Measured with I_F = 0.5A, I_R = 1.0A, I_{rr} = 0.25A.



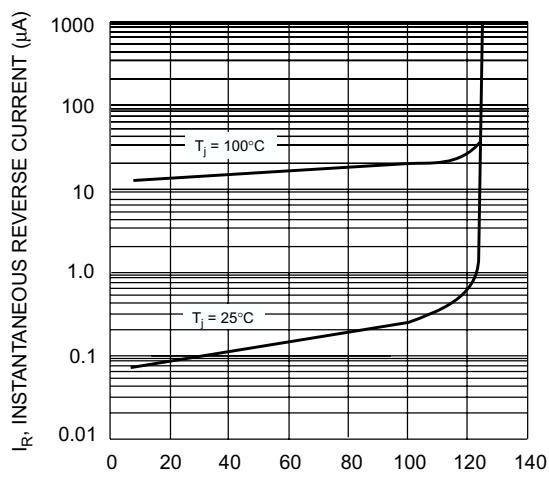
T_T , TERMINAL TEMPERATURE (°C)
Fig. 1 Forward Current Derating Curve



NUMBER OF CYCLES AT 60Hz
Fig. 3 Forward Surge Current Derating Curve



V_F , INSTANTANEOUS FORWARD VOLTAGE (V)
Fig. 2 Typical Forward Characteristics



PERCENT OF RATED PEAK REVERSE VOLTAGE (%)
Fig. 4 Typical Reverse Characteristics

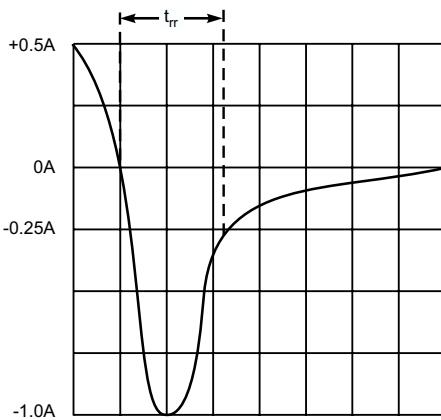
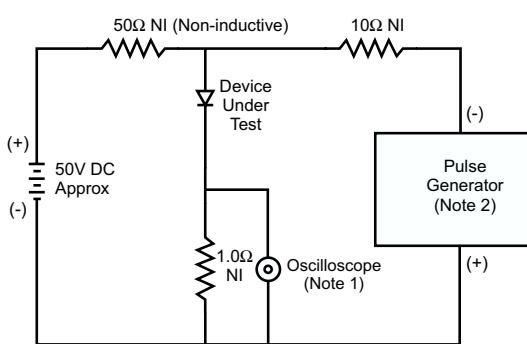


Fig. 5 Reverse Recovery Time Characteristic and Test Circuit